RISC-V Lab

Ex8: Schedule & Review

Content

1. Schedule
2. Group reviews

Schedule

- now: CW24
- final pres: CW31
- **8 weeks** left

Schedule Ex1: Reverse

- 1 weeks reserve / slides / video
- 2 weeks FPGA upload & SW
- 2 weeks system integration, top level timing closure, ...
- 3 weeks
  - module tb
  - module synthesis (!)
  - module / HAL / driver

Do your own !

Schedule: track!